XFBL45(54)1T80DC
10Gb/s BIDI XFP 80km Transceiver

PRODUCT FEATURES

- Hot-pluggable XFP footprint
- Supports 9.95Gb/s to 11.3Gb/s bit rates
- XFI Loopback Mode
- RoHS-6 Compliant (lead-free)
- Up to 80km transmission on SMF
- EEPROM with Serial ID Functionality
- Compliant with XFP MSA with LC connector
- 1490nm EML laser and APD receiver for XFBL451T80DC

  1550nm EML laser and APD receiver for XFBL541T80DC
- Commercial/Industrial Case operating temperature: -10°C to 70°C /-40°C to 85°C
- 2-wire interface with integrated Digital Diagnostic monitoring
- Power dissipation<2.5W

APPLICATIONS

- 10GBASE-BX 10.3125Gb/s Ethernet
- 10GBASE-BX 9.953Gb/s Ethernet
- SONET OC-192 &SDH STM I-64.1

PRODUCT DESCRIPTION

XFBL45(54)1T80DC is hot pluggable Small-Form-Factor transceiver module. It designed expressly for high-speed communication applications that require rates up to 11.3Gb/s, it designed to be compliant with XFP MSA. The module data link up to 80km in 9/125um single mode fiber.

Ordering information

Product part Number	Data Rate (Gbps)	Media	Wavelength (nm)	Transmission Distance(km)	Temperature Range （Tcase）（℃）	
XFBL451T80DC	10.3125	Single mode fiber	1490 TX/1550 RX	80	-10~70	Commercial
XFBL541T80DC	10.3125	Single mode fiber	1550 TX/1490 RX	80	-10~70	Commercial
XFBL451T80DI	10.3125	Single mode fiber	1490 TX/1550 RX	80	-40~85	Industrial
XFBL541T80DI	10.3125	Single mode fiber	1550 TX/1490 RX	80	-40~85	Industrial

Ⅰ.Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	Ts	-40	-	85	ºC	
Relative Humidity	RH	5	-	95	%	
Power Supply Voltage	VCC	-0.3	-	4	V	
Signal Input Voltage	VCC	Vcc-0.3	-	Vcc+0.3	V	

Ⅱ.Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	Tcase	-10	-	70	ºC	Commercial
		-40		85	ºC	Industrial
Supply Voltage – 1.8V supply	Vcc2	1.71		1.89	V	
Supply Voltage – 3.3V supply	Vcc3	3.13		3.47	V	
Supply Current – 1.8V supply	Icc2			200	mA	
Supply Current – 3.3V supply	Icc3			650	mA	
Data Rate	BR	9.95	10.3125	11.3	Gbps	
Transmission Distance	TD	2	-	80	km	
Coupled fiber	Single mode fiber					

Ⅲ. Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Average Launched Power	PO	0	-	4	dBm	XFBL451T80DC
		-1	-	3	dBm	XFBL541T80DC
Average Launch power of OFF transmitter	P_{OFF}	-	-	-45	dBm	Note (1)
Centre Wavelength Range	λC	1480	1490	1500	nm	XFBL451T80DC
		1540	1550	1560	nm	XFBL541T80DC
Side mode suppression ratio	SMSR	30	-	-	dB	
Spectrum Bandwidth(-20dB)	σ	-	-	1	nm	
Extinction Ratio	ER	6		-	dB	Note (2)
Output Eye Mask	Compliant with IEEE 802.3ae requirements					Note (2)
Receiver						
Input Optical Wavelength	λIN	1480	1490	1500	nm	XFBL541T80DC
		1540	1550	1560	nm	XFBL451T80DC
Receiver Sensitivity in average	Psen	-	-	-24	dBm	Note (3)
Input Saturation Power (Overload)	PSAT	-6	-	-	dBm	Note (3)
LOS Assert	LOSA	-38	-	-	dBm	
LOS De-assert	LOSD	-	-	-25	dBm	
LOS -Hysteresis	PHys	0.5	-	4	dB	

Note:
1. The optical power is launched into SMF
2. Measured with RPBS 2^31-1 test pattern @10.3125Gbs
3. Measured with RPBS 2^31-1 test pattern @10.3125Gbs BER=<10^-12

IV. Electrical Interface Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Supply Voltage – 1.8V supply	Vcc2	1.71		1.89	V	
Supply Voltage – 3.3V supply	Vcc3	3.13		3.47	V	
Supply Current – 1.8V supply	Icc2			200	mA	
Supply Current – 3.3V supply	Icc3			650	mA	
Module total power	P			2.5	W	1
XFP Interrupt, Mod_NR	Vol	0		0.4	V	
	Voh	V_{CCHOST} -0.5		V_{CCHOST} +0.3	V	
P_Down/RST	Vil	-0.3		0.8	V	
	Vih	2.0		Vcc3+0.3	V	
Interrupt Assert Delay	Interrupt_on			200	ms	
Interrupt Negate Delay	Interrupt_off			500	us	
Mod_NR Assert / Negate Delay				1	ms	
P-Down reset time		10			us	
Transmitter						
Input differential impedance	R_{in}	80	100	120	Ω	2

Differential data input swing	Vin,pp	120		820	mV	
Transmit Disable Voltage	V_D	2.0		Vcc	V	3
Transmit Enable Voltage	V_{EN}	GND		GND+ 0.8	V	
Receiver						
Differential Output Impedance	Rout	80	100	120	Ω	
Differential data output swing	Vout,pp	340		850	mV	4
Data output rise time	t_r			38	ps	5
Data output fall time	t_f			38	ps	5
LOS Fault	$V_{LOS\ fault}$	Vcc_{HOST} – 0.5		Vcc_{HOST}	V	6
LOS Normal	$V_{LOS\ norm}$	GND		GND+0.5	V	6

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. After internal AC coupling.
3. Or open circuit.
4. Into 100 ohms differential termination.
5. These are unfiltered 20-80% values
6. Loss Of Signal is open collector to be pulled up with a 4.7k – 10kohm resistor to 3.15 – 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.

V. Pin Assignment

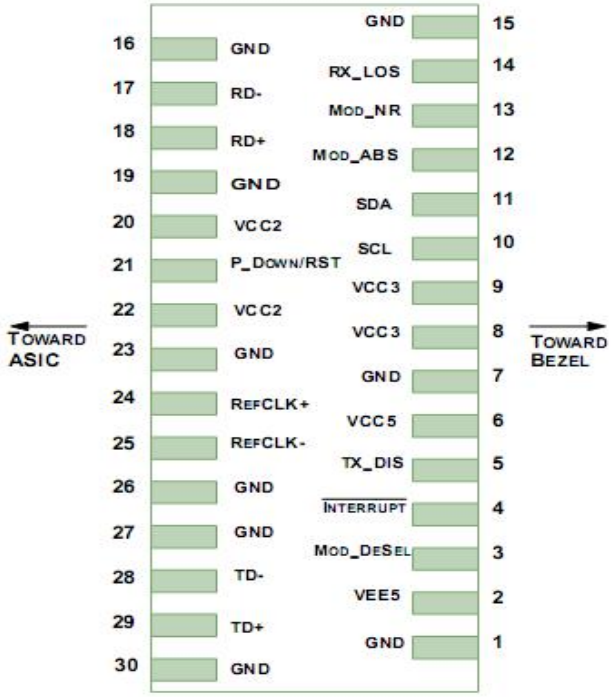


Diagram of Host Board Connector Block Pin Numbers and Name

Pin	Logic	Symbol	Name/Description	Note
1		GND	Module Ground	1
2		VEE5	Optional -5.2 Power Supply – **Not required**	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands	

4	LVTTL-O	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply – **Not required**	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTLI/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTL-O	Mod_NR	Module Not Ready; defines it as a logical OR between RX_LOS and Loss of Lock in TX/RX.	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply	
21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – **Not required**	3
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – **Not required**	3
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10kohms on host board to a voltage between 3.15V and 3.6V.
3. A Reference Clock input is not required by the XFBL-4955(5549)10-80D(A). If present, it will be ignored.

VI. Digital Diagnostic Functions

As defined by the XFP MSA, XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

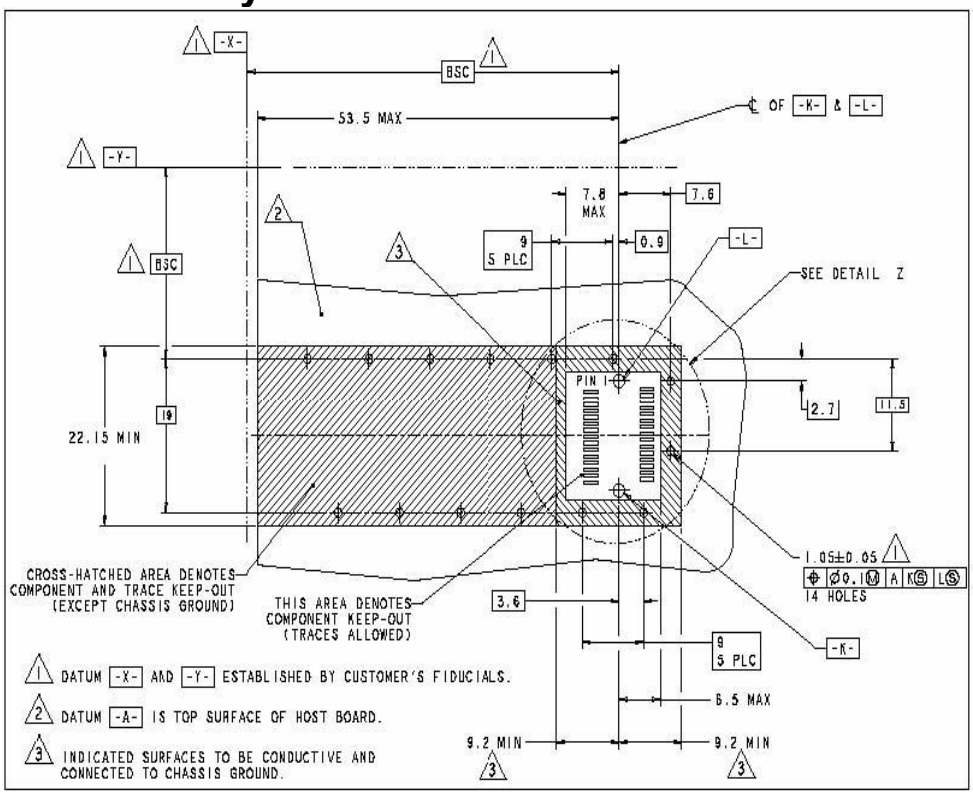
- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

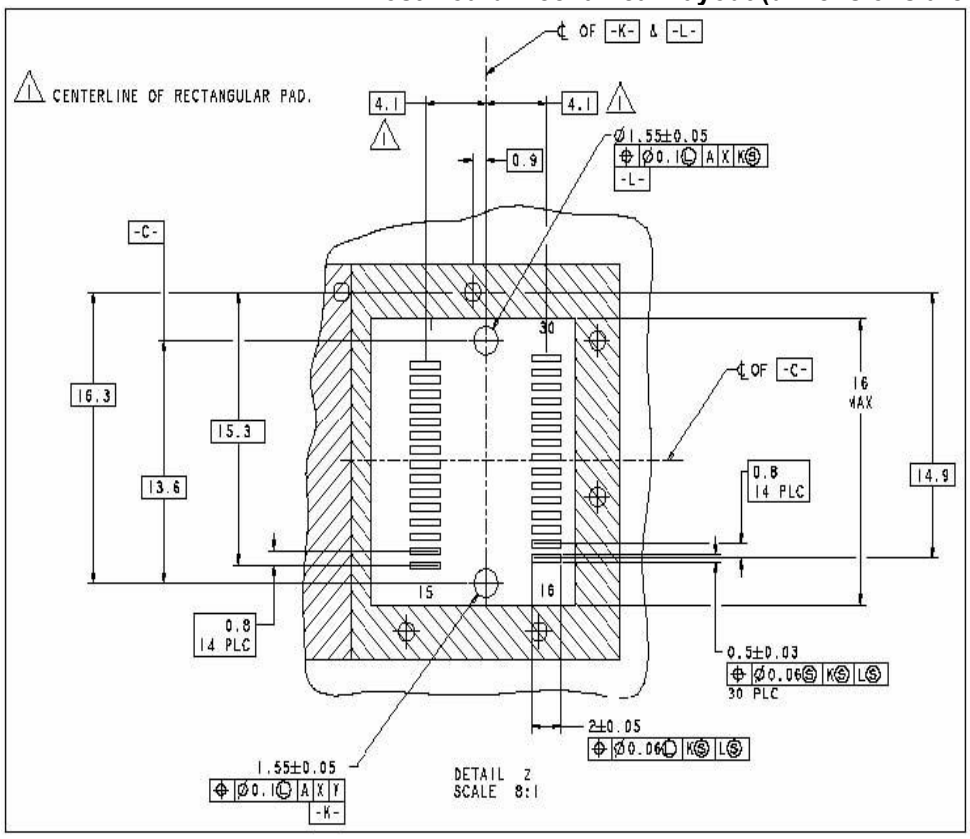
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the XFP MSA Specification.

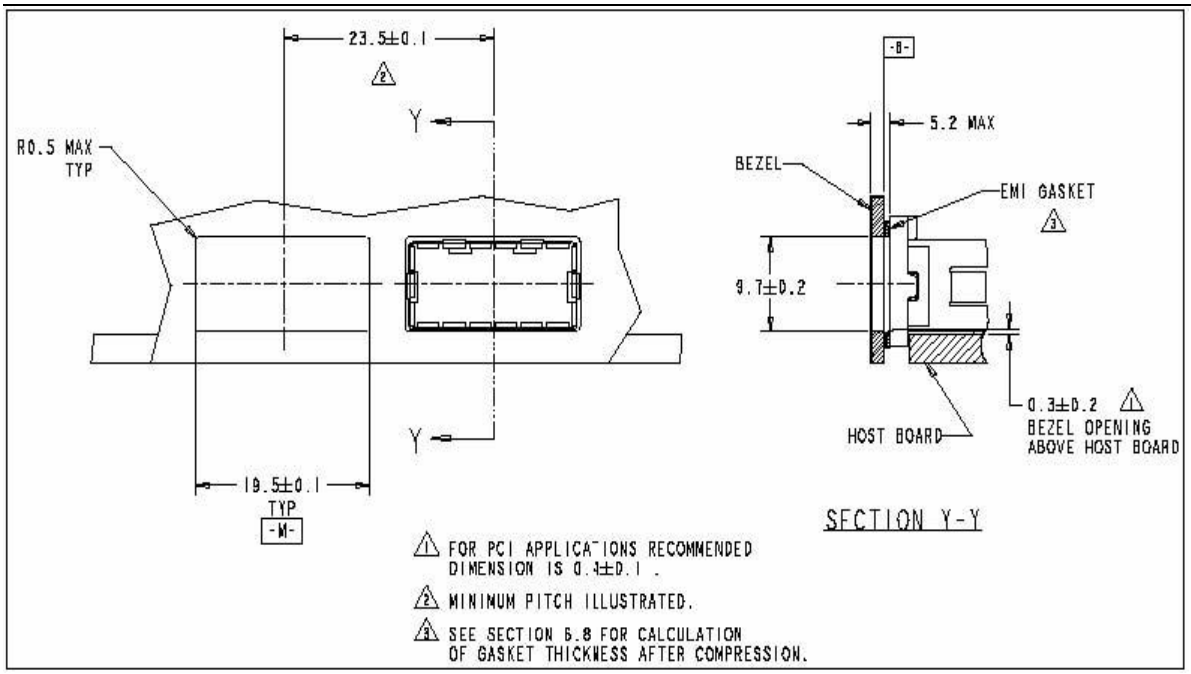
VII. PCB Layout and Bezel Recommendations



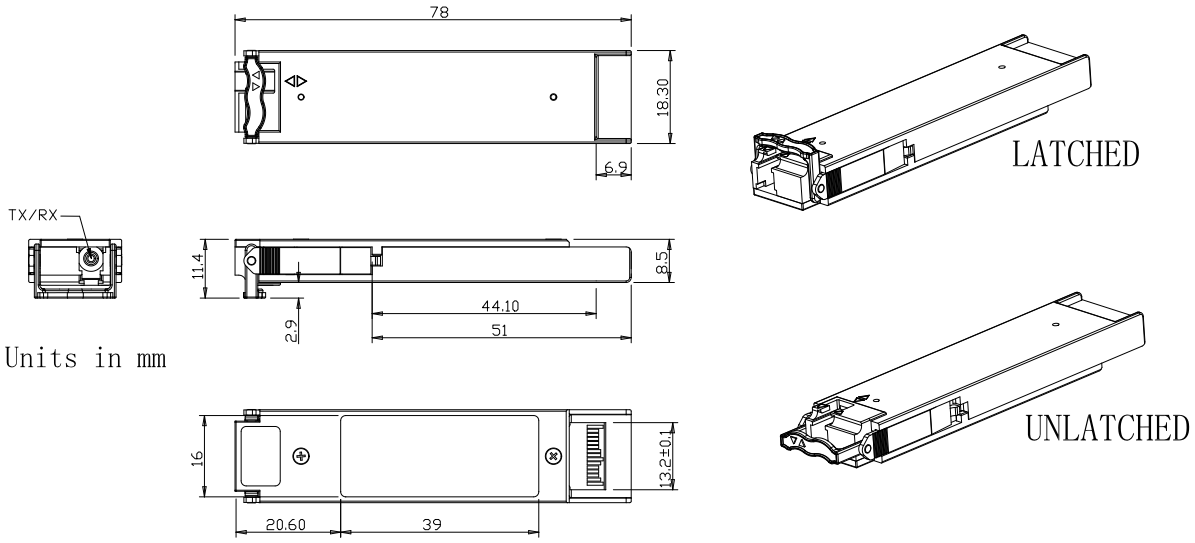
XFP Host Board Mechanical Layout (dimensions are in mm)



XFP Detail Host Board Mechanical Layout (dimensions are in mm)



VIII. Outline Dimensions



IX. Regulatory Compliance

Feature	Reference	Performance
Electrostatic discharge（ESD）	IEC/EN 61000-4-2	Compatible with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN 55022 Class B (CISPR 22A)	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10, 1040.11 IEC/EN 60825-1，2	Class 1 laser product
Component Recognition	IEC/EN 60950 ， UL	Compatible with standards
ROHS	2002/95/EC	Compatible with standards
EMC	EN61000-3	Compatible with standards